Dear All,

Short summary from the 37th HWG Meeting:

We had four presentations regarding the development of readout electronics:

1. M. Idzik reported the status of FLAME chip design. The design is quite advanced and the project should be ready for submission sometime in May. Since we decided recently to move the testbeam of prototype forward calorimeter to ~ middle of 2019. It would be worthwhile to make a dedicated (additional) test-beam at the turn of 2018/2019 for a single plane with FLAME readout to debug and verify its operation.

2. Bartosz Dziedzic reported on the FLAME to FPGA GTP link interface. Main blocks have been developed and verified. Their integration is still needed. In addition Ethernet 1Gbps link is under development. Some adjustments are still needed.

3. Aleksandr Lapkin reported on the status of FPGA development at JINR. Clock Domains Synchronizer was developed. FPGA developments kits have been ordered.

4. Matias Henriquez reported on development of BeamCal readout chip at PUC. Design of 8-channel analog front-end is in progress. It should be submitted at the end of May.

In addition, I have reported that because of probable extension of AIDA2020 project by 1 year, I have asked to delay our FCAL delivery by ~9 months, to have additional safety margin.

Best Regards,

Marek