A short summary from 26th HWG meeting:

1. Yan presented the status of TB2016 analysis

- first studies of noise and signal distribution are ongoing

- for "tracking planes" a reasonable noise is seen

- for calorimeter planes a quite high noise with strange dependence on sensor channel number is seen - to be understood

- first Landau distributions of signals have been obtained

- example event with separated electron and photon has been found

In general, the status is promising, but a lot of work ahead...

2. Itamar gave an update on Moliere radius analysis

- MC energy distribution versus "r" have been calculated and fitted using DD4HEP for different setup and process configurations

- while the data points can be fitted well, for the MC points there is usually a problem in fitting (it looked better for older simulations done with Lucas)

- there was a discussion about how to proceed: whether to continue DD4Hep simulations or to complete the paper on the basis of existing Lucas simulations

- it was agreed that the paper should be updated a.s.a.p. using the existing results and sent to Collaboration

- Collaboration should decide whether the results are satisfactory or more work is needed. If in the meantime more results from DD4Hep are available, it could help in the decision.

3. Marek gave short status on FLAME readout ASIC design

- two main blocks (ASICs): 8 channel FE+ADC and fast serializer have been fabricated quite some time ago

- by know FE, ADC and serializer basic functionality has been positively verified

- what is still waiting and needs update in the test setup is: FE+ADC functionality and precise measurement of eventual error rate for the serializer

- it is not yet known how much time will it take, but the general plan of submission of 16-channel FLAME prototype in the first part of 2017 is still valid

Apart from these presentations, there was a discussion about eventual need of cooling for the LumiCal setup for the next test beams (~1 year from know). Konrad said that CERN could think about, but as a first input an estimation of power consumption is needed. Since the main dissipation will probably come from FPGA readout, which is not yet in advanced stage, such estimation is not yet possible and needs to wait...

Best Regards,
  marek